Functional Verification Methodology and Choices

Course Title

Functional Verification Methodology and Choices

Course Description

Every chip project comes with the challenges of verifying its functional correctness before tapeout. From small to complex highly integrated chips, the project team is confronted with decisions on what verification strategy to use, so as to complete verification within reasonable time frame.

This is especially when there are a number of choices available, from using SystemVerilog (SV) to the increasingly popular Universal Verification Methodology (UVM). To be able to make the best decisions for verification, the fundamentals of each choice should be well understood.

- What are the pros and cons of Verilog/VHDL vs SystemVerilog verification?
- What are the differences between static and object-oriented verification?
- What are the pros and cons of UVM?
- In what types of designs should UVM be used, and designs where you may decide not to use UVM?

To address these questions, a fundamental knowledge of verification methods will be helpful. This course presents overview of some features of SystemVerilog and UVM. Comparisons are then made as to how they are used to implement different verification methods. Next, it will discuss examples of different chip designs to be verified, and choices of methodology to use in each case.

Some of the common myths of SV and UVM will also be discussed.This course also discusses about the general verification flow, with the chip specification being golden, the importance of the testplan, randomization and verification coverages.

Every chip is unique - there is no one-size-fits-all solution to verification. Having a better understanding of the fundamental aspects of SV and UVM verification will assist the team in making better verification decisions.

What You Will Learn

- Better understanding of the choices available for chip verification, and their pros and cons
- New ideas and techniques that you can apply to your current chip verification
- Deeper understanding of the foundations of new verification methodology

Target Audience

This course is intended for a wide range of audiences including:

- Design and verification engineers working on chip functional verification
- Validation engineers working on chip prototyping together with design teams
- Technical managers and directors who manage design and verification engineers
- Chip design teams considering choices of using SV or UVM in verification, and wish to gain more knowledge to help in making decisions
- Anyone who wishes to gain a deeper understanding of the foundations of new verification methodology

Prerequisite

Basics of Verilog/VHDL

Duration

- Company on-site: 1 day (9 a.m. – 5 p.m.)
- Live online training: 2 sessions (9:30 a.m. – 1 p.m)

Course Presentation

Each participant will receive training materials. This course will be presented in lecture style with discussions.

Course Instructor

Chang Chee Keng, Sys-ASIC Designs Pte Ltd

C.K. Chang, B.S.E.E., M.S.E.E., has 30 years of experience in chip design and verification, and has participated in a number of chip development projects. He was a technical staff of AMCC/JNI Corporation (Singapore) and participated in design, verification and architecture of 10Gbit Fibre Channel host adapter ASICs. Prior to that, he founded Digital Media Interconnect Pte Ltd to provide consulting and training services to companies in Singapore and the region. Previous to that, he was a Senior Staff Engineer at Silicon Systems (Singapore) Pte Ltd, a subsidiary of Texas Instruments Inc, and was involved in the design of Firewire storage integrated circuits. Prior to returning to Asia, he worked in Silicon Valley, California, USA, at ESS Technology, 3DO Company and Sun Microsystems in design, verification and architecture of various ASIC development projects.

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Course Contents

Part 1: Overview of Verification (10%)

Typical ASIC Design Flow

Variety of Chip Verification Techniques

Chip Specification as Golden

Verification Engineer's Perspective

Block and System-Level Verification

Verification Testplan and Testbench

History and Goals of SystemVerilog (SV)

History and Goals of UVM

Part 2: Some Aspects of SV Verification (15%)

Directed vs Random Tests

Randomization Scenarios

Scope and Class Randomization

Combining Directed and Random Tests

Functional Simulation

SV Functional Coverage Overview

Code Coverage Overview

Functional Sim vs Code vs Functional Coverage

Part 3: Verification Methodology and Choices (75%)

SystemVerilog Class Overview

Creating Class Instances

Class Inheritance

Interface Overview

Functional Verification Methodology and Choices

- Fully-Static Verification Methodology
- Partial-Object Verification Methodology
- Fully-Object Verification Methodology
- Comparison of Verification Methodologies
- UVM Environment
- UVM Class Hierarchy
- UVM Transactions
- User Sequences
- UVM Component Classes
- UVM Phases
- Bridging UVM to DUT
- Running UVM Test
- TLM Connection Overview
- Scoreboard Overview
- UVM Factory Overview
- Configuration Database Overview
- UVM Register Layer Overview
- Verification Role Partitioning
- Case Examples of DUTs and Verification Choices
- DUT Features and HSSI
- Single vs Multi-Initiators
- Ad-hoc and Standard Interfaces
- SV vs UVM Choices, Internal vs Licensing VIPs
- Some Common Myths of SV and UVM
- Q&A