Universal Verification Methodology (UVM)

Course Title

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Course Description

This course presents Universal Verification Methodology (UVM), its various features and benefits for verification.

Chip designs have grown in complexity and more highly integrated. Many chip designs also require integration of design and verification IPs from external vendors. As a result, functional verification has become more challenging.

UVM has been developed to address issues of verification especially for large complex chips. UVM is an industry standard that defines methods to realize modular, scalable, configurable and reusable verification environments.

Target Audience

This course is intended for those who are involved in digital design verification. They include chip design engineers, verification engineers and technical managers.

Prerequisite

SystemVerilog language, in particular SystemVerilog classes

Duration

- 4 days (9 a.m. – 5 p.m.)

Course Presentation

- Each participant will receive training materials and source code files for lab exercises.
- Lecture is 70%, lab exercises is 30%
- The lab exercises are mostly coded and ready to run. Participants will study and understand the code, run them, and review the outputs and waveforms. In some lab exercises, there will be minor changes to run different scenarios
- Each participant will receive a Certificate of Attendance after completing at least 75% of the course

Course Instructor

Chang Chee Keng, Sys-ASIC Designs Pte Ltd

C.K. Chang, B.S.E.E., M.S.E.E., has 30 years of experience in chip design and verification, and has participated in a number of chip development projects. He was a technical staff of AMCC/JNI Corporation (Singapore) and participated in design, verification and architecture of 10Gbit Fibre Channel host adapter ASICs. Prior to that, he founded Digital Media Interconnect Pte Ltd to provide consulting and training services to companies in Singapore and the region. Previous to that, he was a Senior Staff Engineer at Silicon Systems (Singapore) Pte Ltd, a subsidiary of Texas Instruments Inc, and was involved in the design of Firewire storage integrated circuits. Prior to returning to Asia, he worked in Silicon Valley, California, USA, at ESS Technology, 3DO Company and Sun Microsystems in design, verification and architecture of various ASIC development projects.

Contact

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Course Contents

Course Outline

Day 1:

- Chapter 1: Introduction to UVM
- Chapter 2: Brief Review of SystemVerilog Topics
- Chapter 3: Basics of UVM
- Chapter 4: UVM Reporting
- Chapter 5: Components and Phases (partial)
- Lab Exercises: Labs 1-5

Day 2:

- Chapter 5: Components and Phases (remaining)
- Chapter 6: TLM Connections
- Chapter 7: UVM Scoreboards
- Chapter 8: Transactions
- Chapter 9: Sequences (partial)
- Lab Exercises: Labs 6-10

Day 3:

- Chapter 9: Sequences (remaining)
- Chapter 10: UVM Tests
- Chapter 11: UVM Factory
- Lab Exercises: Labs 11-17, Lab 21
- Appendices A-C

Day 4:

- Chapter 12: Configuration Database
- Chapter 13: Register Layer
- Lab Exercises: Labs 18-20, Labs 22-27