SystemVerilog for Design and Verification

Course Title

SystemVerilog for Design and Verification

Course Description

This course presents the key features of SystemVerilog for design and verification.

SystemVerilog introduces new constructs to enable more robust RTL coding and better compile-time checks compared to Verilog. The language provides a number of new features, such as object-oriented modeling, constrained randomization, functional coverage, assertions and others that enable powerful verification methods for increasingly complex chips.

This course also discusses verification planning, verification strategies (e.g. directed vs random) and choice of SV or UVM methodologies for verification.

SV Assertions for verification will be covered, and an introduction to UVM will be presented.

Target Audience

This course is intended for those who are involved in digital design and verification. They include chip design engineers, verification engineers and technical managers.

Prerequisite

Verilog language

Duration

- 4 days (9 a.m. – 5 p.m.)

Course Presentation

- Each participant will receive training materials and source code for lab exercises
- Please refer to www.sys-asic.com/resources to view the lecture slides and lab workbook
- Lecture is about 70%, lab exercises is 30%
- Each participant will receive a Certificate of Attendance after completing at least 75% of the course

Course Instructor

Chang Chee Keng, Sys-ASIC Designs Pte Ltd

C. K. Chang, B.S.E.E, M.S.E.E, has 30 years of experience in chip development in Asia and USA.

At Sys-ASIC Designs, he provides training and services with a focus on system-level verification, front-end design and verification methodology for ASIC, SoC and FPGA developments. Some of the clients include Nations Technologies, HP Enterprise, A*Star, Silicon Labs, Infineon, and others.

Prior to this, he worked at various companies in Singapore and Silicon Valley, including AMCC/JNI Corporation (Singapore), Silicon Systems (Singapore), ESS Technology, 3DO Company and Sun Microsystems in architecture, design and verification of various ASIC development projects.

Contact

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Course Outline

Day 1:

- Chapter 1: Course Introduction
  - Course Objectives
  - Chip Development Trends
- Chapter 2: Literals and Basic Data Types
  - Literals, Variables and Constants
  - SystemVerilog Data Types
  - 2-State and 4-State types
  - Simulation Time and Timescale
- Chapter 3: Strings and Enumerated Types
  - String Operators and Methods
  - Enumerated Data Types and Methods
- Chapter 4: SystemVerilog Operators
  - Operator Classifications
  - Concatenation and Replication
  - Implicit, Static and Dynamic Casting
- Chapter 5: Assignments and Procedural Statements
  - Blocking and Non-blocking Assignments
  - Continuous Assignments of Nets and Variables
  - Unique and Priority Case
  - Unique and Priority If
  - Loops and Iteration
- Chapter 6: Tasks and Functions
  - Formal Arguments and Data Types
  - Static and Automatic Tasks and Functions
  - Pass By Value and Reference
- Chapter 7: Processes and Control
  - Types of always procedures
  - Types of fork-join statements
  - Procedural Timing Controls

- Event Synchronization and Trigger

Day 2:

- Chapter 8: Arrays and Structures
  - Packed and Unpacked Arrays
  - Dynamic and Associative Arrays
  - Queues and Queue Methods
  - Structures
- Chapter 9: Modules and Hierarchy
  - Compilation Unit and Scope
  - $unit and $root
  - Packages
  - Explicit and wildcard Imports
- Chapter 10: Interfaces
  - Interface with Functionalities
  - Interface with modport
  - Virtual Interface
- Chapter 11: Miscellaneous Constructs
  - Clocking and Program Blocks
  - Semaphore and Mailbox
- Chapter 12: System Tasks and Scheduling Semantics
  - Utility System Tasks and Functions
  - SystemVerilog Event Regions
- Chapter 13: System Verilog Classes
  - Class Declarations and Instances
  - Static Properties and Methods
  - Inheritance
  - Downcasting
  - Overridden Methods and Properties
  - Virtual Methods
  - Virtual Classes
  - Parameterized Classes
  - Traditional vs Object-Oriented Verification

Day 3:

- Chapter 14: Constrained Random Generation
  - Randomization Objectives
  - Scope and Class Randomizations
  - Random Cyclic
  - Constraint Blocks
  - Randomization Controls
  - Random Number Generator and Seeding
- Chapter 15: Functional Coverage

    - Code vs Functional Coverage
    - Coverage Sampling
    - Covergroup and Coverpoints
    - State and Transition Bins
    - Cross Coverage
    - Coverage Computation and Options
- Chapter 16: Verification Planning and Flow
    - Chip Specification as Golden
    - Verification Testplan
    - Combining Directed and Random Testing
- Chapter 17: Direct Programming Interface (DPI)
    - DPI Import and Export
    - Data Type Mapping
    - Bit and Logic Vector
- Chapter 18: Introduction to UVM
    - Main Goals of UVM
    - SystemVerilog and UVM
    - Methodologies Comparison

Day 4:

- Chapter 19: Introduction to SV Assertion
    - Black and White Box Verification
    - Simulation and Formal Methods
    - Immediate and Concurrent Assertions
    - Clock and Sampled Values
- Chapter 20: SVA Constructs
    - Cycle Delay Operator
    - Cycle Delay Range
    - Repetition and Ranges
    - Implication Operators
    - Vacuous Success
    - Property Evaluation Threads
- Chapter 21: Sequence and Property Operations
    - Linear Sequence and Matches
    - Sequence Operators
    - Property Construct
    - Property Operators
- Chapter 22: Assertion Executions
    - SVA Clocking
    - Clock Flow Rules
    - Sampled Value Functions
    - SVA Local Variables
    - Assertion Binding

  - SVA Directives – assert, assume, cover, restrict
  - Assertion Event Scheduling
- Summary of Training
- Q&A