Boundary Scan Architecture (JTAG)

Course Title

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Course Description

This course presents Boundary Scan Architecture (JTAG, IEEE 1149.1) and its benefits in achieving various test goals.

With growing use of more sophisticated chip packaging and Application Specific Integrated Circuits (ASICs), performing in-circuit testing on assembed boards is increasingly challenging, leading to the development of Boundary Scan Architecture (JTAG) as a standardized method for testing chips and boards.

JTAG is also useful for controlling design-for-test (DFT) features of a chip. Virtually every modern chip has now incorporated JTAG technology as part of its DFT strategy and as a debug port.

Target Audience

This course is intended for those who are involved in digital chip and board testing.

They include chip designers, test engineers, production engineers, board designers, product support engineers, application engineers, technical marketing engineers and project managers.

Prerequisite

General familiarity with digital logic. General familiarity with design-for-test and scan-based test techniques is recommended but not required.

Duration

- 1 day (9 a.m. – 5 p.m.)

What You Will Learn

- goals of boundary scan architecture and its benefits over traditional board test techniques.
- architecture of boundary scan such as TAP, TAP controller, instructions and test data registers.
- boundary scan architecture instructions, their operations and usage.
- mandatory and optional features of boundary scan architecture.
- use of boundary scan for sampling system data, bypassing devices, device identification and so on.
- use of boundary scan for assembled board interconnection tests.
- board interconnect fault modeling and board interconnect vector generation.
- use of boundary scan instructions to facilitate testing board with non-boundary scan components.
- use of Boundary Scan Architecture for built-in self test (BIST) and user-specific test features.
- use of Boundary Scan Description Language to automate tests.
- study and examine a real chip with boundary scan architecture implementation.

Course Presentation

Each participant will receive a set of training materials. This training includes quizzes and JTAG software simulation demo to explain the various concepts of the subject. Each participant will receive a Certificate of Attendance after completing at least 75% of the course.

Course Instructor

Chang Chee Keng, Sys-ASIC Designs Pte Ltd

C. K. Chang, B.S.E.E, M.S.E.E, has 30 years of experience in chip development in Asia and USA.

At Sys-ASIC Designs, he provides training and services with a focus on system-level verification, front-end design and verification methodology for ASIC, SoC and FPGA developments. Some of the clients include Nations Technologies, HP Enterprise, A*Star, Silicon Labs, Infineon, and others.

Prior to this, he worked at various companies in Singapore and Silicon Valley, including AMCC/JNI Corporation (Singapore), Silicon Systems (Singapore), ESS Technology, 3DO Company and Sun Microsystems in architecture, design and verification of various ASIC development projects.

Contact

Sys-ASIC Designs Pte Ltd
21 Bukit Batok Crescent
#09-79, WCEGA Tower
Singapore 658065
Tel: (65) 6022 1812
Email: ckchang@sys-asic.com
Website: www.sys-asic.com

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Course Outline

- Assembled Board Testing
- In-Circuit Testing and its challenges
- Boundary-Scan Background
- Multiple Goals of Boundary Scan
- Basic Boundary Scan Architecture
- Test Access Port (TAP)
- TAP Controller and TAP States
- Instruction Register and Operation
- Standard Instructions
- Selected Data Registers
- Mandatory and Optional Features
- BYPASS Instruction
- BYPASS Register Usage
- Boundary Scan Cell Operation Modes
- SAMPLE Instruction
- PRELOAD Instruction
- SAMPLE/PRELOAD Data Flow
- EXTEST Instruction
- EXTEST Data Flow
- EXTEST Board Interconnect Test
- Interconnect Fault Modeling
- Interconnect Test Vectors
- Optional Instructions: CLAMP, HIGHZ, IDCODE, USERCODE
- Device Identification Register
- Initial Chain Integrity Test
- Mixed Boundary-Scan and Non-Boundary Scan Devices
- RUNBIST Instruction
- Concurrent RUNBIST runs
- Built-in Self-Test (BIST) using RUNBIST
- INTEST Instruction
- User-Defined Test Features
- Boundary Scan Description Language (BSDL)
- Hierarchical Scan Description Language
- Review a Chip Specification with JTAG
- JTAG Software Simulation Demo