

Design-for-Test

Course Title

Design-for-Test

Course Description

This course presents fundamentals of Design-for-Test (DFT). As chips grow in complexity and more highly integrated, design-for-test is now accepted as an essential part of the chip design process.

The combined discipline of design and test will require closer working relationship between chip designers and test engineers to achieve the goals of high quality production, lower test costs and meeting time-to-market constraints.

Target Audience

This course is intended for those who wish to gain an understanding of design-for-test (DFT) for digital chips and SoCs (System-on-Chip).

They include chip designers, test engineers, production engineers, board designers, product support engineers, application engineers, technical marketing engineers and project managers.

Prerequisite

General familiarity with digital logic

Duration

- Company onsite training: 2 days (9 a.m. – 5:00 p.m.)
- Live online training: 4 sessions (9:30 a.m. – 1:00 p.m.)

What You Will Learn

- goals of design-for-test and their benefits.
- differences between functional verification and chip testing.
- purposes of fault models and the need for different types of models to achieve test goals.
- ATPG process and techniques used for generating test vectors based on fault models.
- use of fault simulation in ATPG and functional vectors to obtain fault coverage.
- concepts of controllability, observability and testability and how scan design techniques can be used to increase testability of sequential circuits.
- full scan timing procedure and switching between scan and system mode of operation.
- use of multiple scan chain to further reduce test times and its scan timing procedure.
- impact of DFT in chip design area, timing, routing and other practical design issues.
- limitations of stuck-at-fault and the need for other test techniques to supplement scan-based testing.
- functional vector generation to supplement ATPG and ad-hoc methods to increase fault coverage.
- memory fault models and their fault classifications
- memory test algorithms including traditional algorithms and March test algorithms.
- extensions of memory tests from bit-oriented to word-oriented memories
- memory and logic Built-in Self Test (BIST)
- hardware test compression schemes and their use for reducing test times and test data volume.
- I_{DDQ} current testing and future challenges for SoC
- at-speed testing for detecting chip speed and timing problems

Course Presentation

Each participant will receive a set of training materials. The course will include some quizzes to enhance understanding of the subject. There is no lab session for this course.

Each participant will receive a Certificate of Attendance after completing at least 75% of the course.

Course Instructor

Chang Chee Keng, Sys-ASIC Designs Pte Ltd

C.K. Chang, B.S.E.E., M.S.E.E., is a chip designer with over 25 years of experience and has participated in a number of chip development projects. He was a technical staff of AMCC/JNI Corporation (Singapore) and participated in design, verification and architecture of 10Gbit Fibre Channel host adapter ASICs. Prior to that, he founded Digital Media Interconnect Pte Ltd to provide consulting and training services to companies in Singapore and the region. Previous to that, he was a Senior Staff Engineer at Silicon Systems (Singapore) Pte Ltd, a subsidiary of Texas Instruments Inc, and was involved in the design of Firewire storage integrated circuits. Prior to returning to Asia, he worked in Silicon Valley, California, USA, at ESS Technology, 3DO Company and Sun Microsystems in design, verification and architecture of various ASIC development projects.

Contact

Sys-ASIC Designs Pte Ltd

21 Bukit Batok Crescent

#09-79, WCEGA Tower

Singapore 658065

Email: ckchang@sys-asic.com

Website: www.sys-asic.com

Course FAQ

What is the prerequisite to take this course?

Only a general familiarity with digital logic is required.

Who will find this course relevant?

This course will be of interest for a wide range of engineers such as design, test, production and anyone who is involved in chip design and tests.

The course is sometimes conducted for a class with engineers from various engineering departments. Given this diverse group of engineers, the preference is to conduct the course at a pace beneficial for engineers new to DFT.

Design-for-Test

Course Outline

Chip Testing Overview

Goals of Testing Chips
Defect Levels and Escapes
Functional vs. Chip Test
Multiple Test Strategies for System-on-Chip (SoC)
Fault Modeling, Test Generation and Fault Simulation

Defects and Faults
Purpose of Fault Models
Fault Model Characteristics and Types
Stuck-at-Fault

The need for multiple Fault Models
Test Generation Overview
Fault Sensitization/Propagation

Fault Collapsing
Redundant Fault

ATPG Generation Flow

Fault Simulation

ATPG Runtime

Fault Classes

Coverage Statistics

Scan Design Techniques

Non-Scan ATPG complexity
Controllability and Observability
Testability

Effects of Full Scan Designs

Full Scan Test Generation

Timing of Scan Procedure

Scan Methodology Flow

Scan Element Mapping

Full Scan vs. Partial Scan

Impact on Design Area and Timing

Impact on Tester Time

Multiple Clock Domain Design

Multiple Scan Chain Design

Design Issues: Asynchronous Reset, Clock

Logic, Tristate Buses, Datapath Loading

Example Vector Format: TDL

Functional Test Vectors

Functional Verification vs. Chip Test

Functional Test Vector Generation Flow

Functional Module Test

Ad-hoc Methods

Test Logic Selection

ATPG vs Functional Test Vectors

Memory Test and Built-In-Self-Test (BIST)

SRAM Functional Model and Faults

Address Decoder Fault

Memory Cell Fault Classifications

Single Cell Faults and Coupling Faults

Linked Faults and Classification

Static and Dynamic Faults

Zero-One, Checkerboard, WALPAT, GALPAT

March Test Algorithms

March Tests Fault Coverage

Built-in Self Test (BIST)

Memory BIST Architecture

Multiple Input Signature Register (MISR)

Pseudo-Random Pattern Generator (PRPG)

Logic BIST and STUMPS

Test Compression

The Need for Test Compression

Decompressor and Compactor

Linear Decompressors

Broadcast-scan Based Decompressors

Time and Space Compactors

Test Compactor Characteristics

Industry Compression Architectures

I_{DDQ} Current Testing

Limitations of Stuck-at-Fault Model

Static Leakage Current

Defects raising I_{DDQ}

Future Issues of I_{DDQ} Testing for SoCs

At-Speed Testing

Defects Causing Timing Problems

Transition and Path Delay Fault Models

Two Vector Delay Test Sequence

Lumped and Distributed Delays

Static Timing Analysis and Critical Paths

Limitations of Delay Test Models

Scan-Based Delay Testing

Launch-Off-Shift Test Method

Launch-Off-Capture Test Method