

Public Training Courses:

Course	Fee (no GST)	Closing Date	Course Dates
Design for Test (DFT)	S\$1,450	29 June 2026	13-15 July 2026
SystemVerilog for Design and Verification (SV)	S\$1,950	6 July 2026	20, 22, 24, 27 July 2026
Universal Verification Methodology (UVM)	S\$1,950	20 July 2026	3, 5, 7, 11 Aug 2026

Registration Form:

Details of Participants			
	1 st Participant	2 nd participant	3 rd participant
Course Title			
Course Date			
Participant's Name			
Designation & Dept			
Participant's Email			
Tel. No.			
Company Authorisation Details			
Contact Person			
Designation & Dept			
Contact Person's Email			
Tel No.			
Company			
Address			

 Authorised Signature
 Name:
 Designation:

 Date:

Registration:

- Please complete the registration form, and email a scanned form to ckchang@sys-asic.com
- For confirmation of registration, payment must be received at least 10 days prior to course commencement
- You will receive an email confirming your registration upon payment

Payment Methods:

- PayNow UEN: 201215347C
- Bank Transfer
- Cheque payable to Sys-ASIC Designs Pte. Ltd.

Course Venue:

- To be announced later

Refund and Cancellation:

- Payment will be refunded in full for cancellation received in writing at least 10 working days prior to course commencement
- No refund for cancellation less than 10 working days from course commencement or for no-show occurrence
- Substitution of participants will be accepted prior to course commencement
- Sys-ASIC Designs reserves the right to cancel or reschedule a course at any time, e.g. due to low enrollment or other unforeseen circumstances. Every effort will be made to inform participants promptly of the change. If a course is cancelled, payment for registration will be refunded in full